Amendments to the Claims:

Please note that all claims currently pending and under consideration in the referenced application are shown below. This listing of claims will replace all prior versions and listings of claims in the application.

Please amend claims 7 and 10 as set forth hereinbelow.

Listing of Claims:

1. (Previously Presented) An integrated circuit package comprising:

a semiconductor die;

a plurality of conductive elements arranged in an array, the array including at least a first set of spaced and electrically isolated conductive elements adjacent an outer lateral periphery of the integrated circuit package and at least one other set of spaced and electrically isolated conductive elements inwardly adjacent the at least a first set of conductive elements, the at least one other set of conductive elements being located outside a lateral periphery of the semiconductor die;

a dielectric encapsulant formed over the semiconductor die and defining the outer lateral periphery of the integrated circuit package, the dielectric encapsulant extending at least partially laterally about the plurality of conductive elements and leaving an outer surface of each conductive element exposed; and

a recess in the dielectric encapsulant between at least one conductive element of the at least a first set of conductive elements and at least one adjacent conductive element of the at least one other set of conductive elements.

2. (Original) The integrated circuit package of claim 1, wherein the semiconductor die includes a plurality of bond pads and wherein each of the plurality of bond pads is electrically connected with a conductive element of the plurality of conductive elements.

3. (Original) The integrated circuit package of claim 2, wherein the electrical connection between each of the plurality of bond pads and each respective conductive element of the plurality of conductive elements includes a wire bond.

4. (Original) The integrated circuit package of claim 1, wherein the conductive elements of the at least a first set of conductive elements are substantially aligned with the conductive elements of the at least one other set of conductive elements transverse to an adjacent outer lateral peripheral edge of the integrated circuit package.

5. (Original) The integrated circuit package of claim 4, wherein the conductive elements of the at least a first set of conductive elements are offset relative to the conductive elements of the at least one other set of conductive elements.

6. (Original) The integrated circuit package of claim 1, wherein the recess comprises an elongated, trough-like recess extending substantially between conductive elements of the at least a first set and conductive elements of the at least one other set disposed along a common laterally outer peripheral edge of the integrated circuit package.

7. (Currently Amended) A semiconductor die assembly, comprising:

a semiconductor die having a plurality of bond pads;

a lead frame having a plurality of conductive leads, each conductive lead being electrically coupled at spaced locations on the conductive lead to at least two bond pads of the plurality of bond pads; and

a severance region defined on each conductive lead, the severance region being located and configured to facilitate separation of its associated conductive lead into at least two mutually electrically isolated conductive elements such that each of the at least two mutually electrically isolated conductive elements comprise at least one of the spaced locations to which a bond pad of the at least two bond pads are electrically coupled.

8. (Original) The semiconductor die assembly of claim 7, further comprising a dielectric encapsulant formed about the semiconductor die and partially about the lead frame.

9. (Previously Presented) The semiconductor die assembly of claim 7, further comprising a wire bond coupling each conductive lead at the spaced locations thereon to one of the at least two bond pads of the plurality of bond pads.

10. (Currently Amended) The semiconductor die assembly of claim 9, wherein the severance region of each conductive lead includes at least one notch formed in a surface thereof ~~each conductive lead includes a severance region configured to facilitate separation thereof into at least two mutually electrically isolated conductive elements~~.

11. (Previously Presented) A memory module comprising:

a module board configured to be electrically coupled with a higher level of packaging; and

at least one integrated circuit package electrically coupled with the module board, the at least one integrated circuit package comprising:

a semiconductor die;

a plurality of conductive elements arranged in an array, the array including at least a first set of spaced and electrically isolated conductive elements adjacent an outer lateral periphery of the at least one integrated circuit package and at least one other set of spaced and electrically isolated conductive elements inwardly adjacent the at least a first set of conductive elements, the at least one other set of conductive elements being located outside a lateral periphery of the semiconductor die;

a dielectric encapsulant formed over the semiconductor die and defining the outer lateral periphery of the at least one integrated circuit package, the dielectric encapsulant extending at least partially laterally about the plurality of conductive elements and leaving an outer surface of each conductive element exposed; and

a recess in the dielectric encapsulant between at least one conductive element of the at least a first set of conductive elements and at least one adjacent conductive element of the at least one other set of conductive elements.

12. (Previously Presented) A computer system comprising:

an input device;

an output device;

a processor coupled to the input and output devices; and

a memory module coupled to the processor, the memory module comprising a module board coupled to at least one integrated circuit package comprising:

a semiconductor die;

a plurality of conductive elements arranged in an array, the array including at least a first set of spaced and electrically isolated conductive elements adjacent an outer lateral periphery of the at least one integrated circuit package and at least one other set of spaced and electrically isolated conductive elements inwardly adjacent the at least a first set of conductive elements, the at least one other set of conductive elements being located outside a lateral periphery of the semiconductor die;

a dielectric encapsulant formed over the semiconductor die and defining the outer lateral periphery of the at least one integrated circuit package, the dielectric encapsulant extending at least partially laterally about the plurality of conductive elements and leaving an outer surface of each conductive element exposed; and

a recess in the dielectric encapsulant between at least one conductive element of the at least a first set of conductive elements and at least one adjacent conductive element of the at least one other set of conductive elements.

13. (Previously Presented) A semiconductor die assembly, comprising:

a semiconductor die having a plurality of bond pads on an active surface thereof;

at least one set of mutually spaced conductive elements laterally outboard of at least one peripheral edge of the semiconductor die, and at least another set of mutually spaced conductive elements spaced from and laterally outboard of the at least one set of conductive elements;

a plurality of wire bonds extending between bond pads of the plurality and conductive elements of the at least one set and the at least another set; and

a package comprising dielectric material extending over the semiconductor die and the plurality of wire bonds and having an outer lateral periphery substantially coincident with outer lateral extents of the at least another set of conductive elements, dielectric material of the package extending at least partially about each of the conductive elements of the at least one set and the at least another set and leaving a surface thereof exposed.

14. (Original) The semiconductor die assembly of claim 13, further comprising a die paddle to which the semiconductor die is secured by a back side thereof.

15. (Original) The semiconductor die assembly of claim 13, wherein the at least one set of conductive elements and the at least another set of conductive elements extend around a plurality of peripheral edges of the semiconductor die.

16. (Original) The semiconductor die assembly of claim 13, wherein the at least one set of conductive elements and the at least another set of conductive elements extend around four peripheral edges of the semiconductor die.

17. (Original) The semiconductor die assembly of claim 13, further including an elongated, trough-like recess extending between conductive elements of the at least one set and conductive elements of the at least another set and substantially parallel to the at least one peripheral edge of the semiconductor die.

18. (Previously Presented) The semiconductor die assembly of claim 13, wherein the exposed surfaces of the conductive elements of the at least one set and the at least another set are oriented substantially parallel to the active surface of the semiconductor die.

19. (Previously Presented) The semiconductor die assembly of claim 7 wherein the plurality of conductive leads extend substantially perpendicular an adjacent outer lateral peripheral edge of the semiconductor die.

20. (Previously Presented) The semiconductor die assembly of claim 7 wherein the plurality of conductive leads extend around a plurality of peripheral edges of the semiconductor die.